

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/668,745

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Title: METHOD AND APPARATUS FOR PROVIDING AN INTEGRATED PRINTED CIRCUIT BOARD REGISTRATION COUPON

Assignee: Intel Corporation

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Dkt: 884.942US1 (INTEL)

IN THE DRAWINGS

Corrected drawings are supplied herewith, each labeled as "REPLACEMENT SHEET".

REMARKS

This responds to the Office Action mailed on January 24, 2006. In this response, claims 1, 5, 6, 10, 16 and 28-30 are amended. Claims 31-33 are added. No claims are canceled. As a result, claims 1-16 and 28-33 are now pending in this application.

Objection of the Claims

Rejection: Claims 1, 5, 6, 10 and 29-30 were objected to on the basis of a number of informalities specified by the Examiner.

Response: The various claims informalities were corrected as required by the Examiner.

§102 Rejection of the Claims

Rejection: Claims 1-16 and 28-30 were rejected under 35 USC § 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842).

Response: Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, “[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*” *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Claim 1 now recites “...a plane metallization layer within the device; and a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer, and electrically isolated from the plurality of component mounting pads, the plated through hole and one of the component mounting pads adapted to receive a circuit tester to test the spacing of a

plane metallization layer from a signal through hole that passes through the plane metallization layer.” The Brinthaup, III et al. (U.S. 6,521,842) reference fails to teach the claim as now amended. Brinthaup, III et al. (U.S. 6,521,842) fails to teach a component mounting pad and a plated through hole adapted to receive a testing apparatus to test the spacing between a plane metallization layer and a signal through hole that passes through the plane metallization layer. In the Brinthaup, III et al. (U.S. 6,521,842) reference, each of the plated through holes 110A, 110B and 110C is connected to one or more ground planes (See column 2, lines 11-18). Pins 170A, 170B and 170C connected to each of the plated through holes 110A, 110B and 110C, respectively. There is no teaching in the Brinthaup, III et al. (U.S. 6,521,842) reference of signal through hole that passes through the plane metallization layer, as now recited in the claim. The Brinthaup, III et al. (U.S. 6,521,842) reference rather teaches:

“A plurality of signal lines 150 are dispersed between power planes 121 through 132 in a plurality of signal planes 155. **Signal planes 155 are separated from power planes 121 through 132 by dielectric material.** In one example the “sandwich” structure of PCB 100 may be formed by etching a signal plane on one side and a power plane on the other side of a printed circuit board joining multiple boards with epoxy or other dielectric adhesive, wherein the dielectric material is epoxy/glass material, fluropolymer, allylated polyphenyl esters, cyanate ester epoxy, (i.e. epoxy, PTFE, or other known dielectric) on one side of signal lines 150 and epoxy or other dielectric adhesive known in the art on the other side of the signal lines.” (Emphasis added) (See column 2, lines 18-30 of Brinthaup, III et al.).

In short, the Brinthaup, III et al. (U.S. 6,521,842) reference fails to teach a signal through hole that passes through the plane metallization layer, since all the signal planes are sandwiched between power planes. In addition, there is no teaching in the Brinthaup, III et al. (U.S. 6,521,842) reference of a component mounting pad adapted to receive a circuit tester to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer. In fact the figures in the Brinthaup, III et al. (U.S. 6,521,842) reference only show the pins associated with the power planes and the specific electrical attachment or isolation with respect to the various power planes 121-132. The same appears to be true with the embodiments shown in FIGs. 5-14 which show the the specific electrical attachment or isolation with respect to the various power planes as well as thermal breaks, bridges to the plated through holes of interest, and thermal vents. As a result, claim 1, as now amended, now overcomes the

Examiner's rejection under 35 U.S.C. 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842).

Claims 2-9 depend, directly or indirectly, from claim 1 and include its limitations by their dependency. As a result, the rejection of claims 2-9 under 35 USC § 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842) is now also overcome.

Claim 10 now recites "...a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including [[a]] the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads; and a signal carrying through hole passing through and spaced away from the plane metallization layer, attached to a pad at one of the first major exterior surface and the second major exterior surface." As argued above, the Brinthaup, III et al. (U.S. 6,521,842) reference fails to teach a signal through hole that passes through the plane metallization layer, since all the signal planes are sandwiched between power planes. As a result, claim 10, as now amended, now overcomes the Examiner's rejection under 35 U.S.C. 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842).

Claims 11-16 directly depend from claim 10 and include its limitations by their dependency. As a result, the rejection of claims 11-16 under 35 USC § 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842) is now also overcome.

Claim 28 recites "...a plated through hole attached to a plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer within the device, and electrically isolated from the plurality of component mounting pads, wherein the feature positioned within the device passes through the plane metallization layer and is isolated from the plane metallization layer; and a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer." As argued above, the Brinthaup, III et al. (U.S. 6,521,842) reference fails to teach a feature passing through the plane metallization layer. In addition, there is no teaching of a testing device in the Brinthaup, III et al. (U.S. 6,521,842) reference. As a result, claim 28,

as now amended, now overcomes the Examiner's rejection under 35 U.S.C. 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842).

Claims 28 and 29 directly depend from claim 28 and include its limitations by their dependency. As a result, the rejection of claims 28 and 29 under 35 USC § 102(e) as being anticipated by Brinthaup, III et al. (U.S. 6,521,842) is now also overcome.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6977) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24th day of April, 2006.

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